REMARKS

Claims 1-3, 6-10, 13-15 and 19-23 have been amended. No claims have been added or cancelled. Therefore, claims 1-23 remain pending in the application. Reconsideration is respectfully requested in light of the following remarks.

Title:

The Examiner objected to the title of the invention as not being descriptive. Applicant traverses this objection. The Examiner submits that a new title is required that is clearly indicative of the invention to which the claims are directed. However, the current title, "Instruction Cache Prefetch Based on Trace Cache Eviction", is clearly indicative of the claimed invention. Applicants' claim 1 recites, "the prefetch unit is configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache." Thus, the title is clearly descriptive of what is recited in claim 1.

Section 102(b) Rejection:

The Examiner rejected claims 1, 6-8, 13-18 and 23 under 35 U.S.C. § 102(b) as being anticipated by Mendelson et al. (U.S. Publication 2002/0095553) (hereinafter "Mendelson"). Applicants respectfully traverse this rejection for at least the following reasons.

Regarding claim 1, contrary to the Examiner's assertion, Mendelson fails to teach or suggest *the prefetch unit is configured to fetch instruction code from a system memory for storage within the instruction cache, and wherein the prefetch unit is further configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache.* First, the Examiner asserts that the L2 cache of Mendelson stores instructions and is, thus, analogous to the instruction cache of

Applicants' claim 1. However, L2 cache 340 of Mendelson is a second-level trace cache, that may be added to trace cache subsystem 120, and that is distinguished from a traditional L2 cache in that the L2 trace-cache 340 contains traces whereas a traditional L2 cache contains data or instructions that have not been built into a trace. (See, e.g., paragraphs [0036] – [0037]). Thus, L2 trace-cache 340 is not an instruction cache, as would be understood by one of ordinary skill in the art, but a trace cache. The system of Mendelson does, however, include an instruction cache, specifically an L1 instruction cache. This instruction cache is illustrated as cache memory 140 of FIG. 1C (see, e.g., paragraph [0020].)

The Examiner further submits that the Cache Manager 310 of Mendelson is analogous to Applicants' prefetch unit. Applicants assert, however, that Cache Manager 310 is clearly not the same as the prefetch unit of Applicants' claim 1. First, the Cache manager is clearly not configured to fetch instruction code from a system memory for storage within the instruction cache, as recited in claim 1. Furthermore, a prefetch unit, such as that of Applicants' claim 1, is well-known in the microprocessor art and one of ordinary skill in the art at the time the invention was made would not consider Cache Manager 310 of Mendelson to be a prefetch unit.

The Examiner submits that L2 cache 340, Cache Manager 310, and paragraph [0039] of Mendelson disclose *wherein the prefetch unit is configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache.* The Examiner asserts, "the management logic fetches instruction traces to the L2 cache in response to their being evicted from a higher-level trace cache 320 or 330." While this paragraph does describe that traces evicted from FTC 320 or MTC 330 are transferred for storage in the L2 trace cache (under control of Cache Manager 310), this has nothing to do with a prefetch unit fetching a line of instructions into the instruction cache in response to a trace being evicted from the trace cache. First, as discussed above, Cache Manager 310 is clearly not a prefetch unit, according to the limitations recited in Applicants' claim 1. Second, Cache Manager 310 does not move anything into the instruction cache (cache 140 of Mendelson), but instead transfers a trace entry into

another trace cache (Mendelson's L2 trace cache). In addition, Cache Manager 310 does not fetch a line of instructions (such as would be stored in system memory), in response to a trace being evicted, but instead transfers the evicted trace entry itself from one trace cache to another.

Applicants note that a mechanism, similar to Mendelson's, for transferring an evicted trace to another level of trace cache is described in the specification of the present invention (see, e.g., paragraphs [0046]-[0047]). However, this mechanism is clearly not the subject matter of Applicants' claim 1, in which *the prefetch unit, that is configured to fetch instruction code from a system memory for storage within the instruction cache, fetches a line of instructions into the instruction cache in response to a trace being evicted from the trace cache.*

Applicants remind the Examiner that anticipation requires the presence in a single prior art reference disclosure of each and every limitation of the claimed invention, arranged as in the claim. M.P.E.P 2131; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The **identical** invention must be shown in as complete detail as is contained in the claims. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). As discussed above, Mendelson fails to disclose *the prefetch unit is configured to fetch instruction code from a system memory for storage within the instruction cache, and wherein the prefetch unit is further configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache.* Therefore, Mendelson cannot be said to anticipate claim 1.

For at least the reasons above, the rejection of claim 1 is not supported by the cited art and removal thereof is respectfully requested.

Claim 8 includes limitations similar to claim 1, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 6, contrary to the Examiner's assertion, Mendelson fails to teach or suggest *the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response to the eviction of certain traces from the trace cache if the line of instructions is already stored in the instruction cache.* The Examiner asserts that if an instruction trace is already stored in the L2 cache, it cannot be evicted from the trace cache, and hence, will not be refetched by the L2 cache. However, claim 6 recites what the prefetch unit is configured to do in response to the eviction of certain traces. Therefore, the Examiner's remarks about what happens when a trace in Mendelson is not evicted do not apply to claim 6.

For at least the reasons above, the rejection of claim 6 is not supported by the cited art and removal thereof is respectfully requested.

Claims 13 and 17 include limitations similar to claim 6, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 7, contrary to the Examiner's assertion, Mendelson fails to teach or suggest *the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response to the eviction of certain traces from the trace cache if the evicted trace is predicted unlikely to re-execute.* The Examiner asserts that Mendelson's use counter is a method of indicating if a trace is likely to be re-used (paragraph [0040], lines 5-7). While this is true, the response in Mendelson to predicting that a trace is unlikely to re-execute is not to *inhibit the fetch of a line of instructions into the instruction cache*, as in claim 7. As discussed above, the system of Mendelson is not configured to fetch a line of instructions into the instruction cache in response to a trace eviction. It is also not configured to inhibit such a fetch in response to eviction of certain traces. Instead, in Mendelson, the response to predicting that a trace is unlikely to re-execute is to discard the trace (see, e.g., FIG. 5).

For at least the reasons above, the rejection of claim 7 is not supported by the cited art and removal thereof is respectfully requested.

Claims 14 and 18 include limitations similar to claim 7, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 15, contrary to the Examiner's assertion, Mendelson fails to teach or suggest *evicting a trace from a trace cache* and *fetching a line of instructions into an instruction cache from a system memory in response to said evicting*. The Examiner again cites paragraph [0039], lines 3-6 as teaching these limitations. However, as discussed above, Mendelson does not disclose fetching a line of instructions, or fetching them into an instruction cache from a system memory, as recited in claim 15. Instead, Mendelson describes transferring an evicted trace entry itself from one trace cache to another trace cache. Therefore, Mendelson cannot be said to anticipate claim 15.

For at least the reasons above, the rejection of claim 15 is not supported by the cited art and removal thereof is respectfully requested.

Claim 23 includes limitations similar to claim 15, and so the arguments presented above apply with equal force to this claim, as well.

Regarding claim 16, contrary to the Examiner's assertion, Mendelson fails to teach or suggest *checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace*. The Examiner asserts that the processor must inherently check if a trace is already stored in the L2 cache before storing it and that storing the same trace cache more than once in the L2 cache is a waste of resources. Applicants respectfully disagree. First, Applicants' claim does not recite checking a trace cache (such as Mendelson's L2) for lines of instructions comprising the instructions corresponding to the evicted trace, but instead recites checking the instruction cache (Mendelson's cache memory 140).

Furthermore, there is nothing inherent about checking any memory (including an

instruction cache or a trace cache) to see if an item is already stored there before storing it. Applicants remind the Examiner that to establish inherency, it must be "clear that the missing descriptive matter is **necessarily present** in the things described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPA2d 1949, 1950-51 (Fed. Cir. 1999) (emphasis added). The Examiner has provided no such evidence, and, in fact, his assertion is incorrect. As would be clear to one of ordinary skill in the art at the time the invention was made, in various embodiments of a computer system or its memory systems, there may be many valid reasons for storing a duplicate copy of something in a memory, such as to provide redundancy, or to optimize the system for speed of storing data (such as by storing data without such checking) rather than for memory utilization (not "wasting resources"), just to name two.

Since Mendelson does not teach or suggest *checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace*, and it has been shown that this is not inherent in the implementation of a trace cache or instruction cache, Mendelson cannot be said to anticipate claim 16.

For at least the reasons above, the rejection of claim 16 is not supported by the cited art and removal thereof is respectfully requested.

Section 103(a) Rejection:

The Examiner rejected claims 2-5, 9-12 and 19-22 under 35 U.S.C. § 103(a) as being unpatentable over Mendelson. Applicants traverse this rejection for at least the following reasons.

Regarding claim 2, contrary to the Examiner's assertion, Mendelson does not teach or suggest *the prefetch unit is configured to fetch a line into the instruction cache*

comprising instructions that correspond to operations that precede a branch in the evicted trace. The Examiner takes Official Notice that traces may consist of multiple branches and asserts that if a trace has two or more branch instructions in it, it is guaranteed to have at least one instruction which precedes a branch instruction. Applicants assert, however, that claim 2 recites fetching a line into the instruction cache (Mendelson's cache memory 140) comprising instructions that correspond to operations that precede a branch in the evicted trace, which the system of Mendelson does not do. Instead, Mendelson discloses transferring an evicted trace from one trace cache to another trace cache. Therefore, the Examiner's remarks do not apply to claim 2, regardless of the contents of the evicted trace.

Applicants remind the Examiner that to establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Mendelson clearly does not teach or suggest *the prefetch unit is configured to fetch a line into the instruction cache comprising instructions that correspond to operations that precede a branch in the evicted trace.*

For at least the reasons above, the rejection of claim 2 is not supported by the cited art and removal thereof is respectfully requested.

Claims 9 and 19 include limitations similar to claim 2, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 3, contrary to the Examiner's assertion, Mendelson does not teach or suggest *the prefetch unit is configured to fetch a line into the instruction cache comprising instructions that correspond to operations that follow a branch in the evicted trace.* The Examiner takes Official Notice that traces may consist of multiple branches and asserts that if a trace has two or more branch instructions in it, it is guaranteed to have at least one instruction which follows a branch instruction. Applicants assert, however, that claim 3 recites fetching a line into the instruction cache (Mendelson's

cache memory 140) comprising instructions that correspond to operations that follow a branch in the evicted trace, which the system of Mendelson does not do. Instead, Mendelson discloses transferring an evicted trace from one trace cache to another trace cache. Therefore, the Examiner's remarks do not apply to claim 3, regardless of the contents of the evicted trace.

For at least the reasons above, the rejection of claim 3 is not supported by the cited art and removal thereof is respectfully requested.

Claims 10 and 20 include limitations similar to claim 3, and so the arguments presented above apply with equal force to these claims, as well.

Regarding claim 4, the Examiner admits that Mendelson fails to disclose *wherein the prefetch unit is configured to prefetch a plurality of lines of instructions into the instruction cache in response to the trace being evicted from the trace cache.* The Examiner takes Office notice that traces commonly consist of multiple lines when stored in a cache. Applicants assert, however, that claim 4 recites *prefetching a plurality of lines of instructions into the instruction cache* (Mendelson's cache memory 140) *in response to the trace being evicted from the trace cache*, which the system of Mendelson does not do. Instead, Mendelson discloses transferring an evicted trace from one trace cache to another trace cache. Therefore, the Examiner's remarks do not apply to claim 4, regardless of the contents of the evicted trace or the number of lines in which it is stored.

For at least the reasons above, the rejection of claim 4 is not supported by the cited art and removal thereof is respectfully requested.

Claims 11 and 21 include limitations similar to claim 4, and so the arguments presented above apply with equal force to these claims, as well.

Applicants assert that numerous other ones of the dependent claims recite further distinctions over the cited art. However, since the rejection has been shown to be

unsupported for the independent claims, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicants submit the application is in condition for allowance, and prompt notice to that effect is respectfully requested.

If any extension of time (under 37 C.F.R. § 1.136) is necessary to prevent the above-referenced application from becoming abandoned, Applicants hereby petition for such an extension. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-91600/RCK.

Also enclosed herewith are the following items:

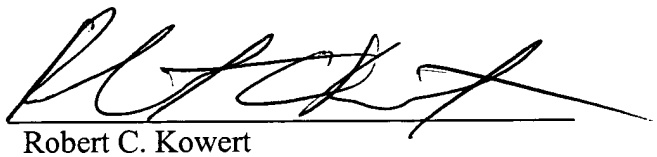
☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Notice of Change of Address

☐ Other:

Respectfully submitted,



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